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METHOD AND APPARATUS FOR SWITCHING DATA BETWEEN BITSTREAMS OF A CIRCUIT SWITCHED TIME DIVISION MULTIPLEXED NETWORK

Technical field of the invention

The present invention refers to a method and an apparatus for switching data at least from a first bitstream to a second bitstream of a circuit switched time division multiplexed network, each of said bitstreams being divided into cycles and each of said cycles being divided into time slots.

Technical Background and Prior Art

Today, new types of circuit-switched communication networks are being developed for the transfer of information using synchronous or isochronous, time division multiplexed bitstreams, wherein a bitstream is divided into cycles, each cycle in turn being divided into time slots.

An example of such a network is described in "The DTM Gigabit Network", Christer Bohm, Per Lindgren, Lars Ramfelt, and Peter Sjödin, Journal of High Speed Networks, 3(2):109-126, 1994, and in "Multi-gigabit networking based on DTM", Lars Gauffin, Lars Håkansson, and Björn Pehrson, Computer networks and ISDN Systems, 24(2), 119-139, April 1992.

The basic topology of a network of this kind is preferably a bus with two unidirectional, multi-access optical fibers connecting a number of nodes, each node being arranged to serve one or more end users connected thereto. Note, however, that the topology may just as well be realized by any other kind of structure, e.g. a ring structure or a hub structure.

The bandwidth of each wavelength on the bus, i.e. each bitstream on each fiber, is divided into fixed length cycles which in turn are divided into fixed size time slots. The number of slots in a cycle thus depend on the network's bit-rate. The time slots are divided into

two groups, control slots and data slots. Control slots are used for transferring of signaling messages between said nodes for the network's internal operation. The data slots are used for the transfer of data between said users connected to the different nodes.

Each node is arranged to dynamically allocate time slots for its respective end users to use when sending or receiving information to or from other users. As a result, different end users have write access to different data slots.

When, for example, a first user connected to a first node wants to transfer information to a second user connected to a second node, said first node will allocate a number of data slots within each cycle for the first user to write data into. The first node will also send a control message in a control slot to the second node, instructing said second node to read any data being provided in said allocated data slots within said cycle and to send such data to said second user. Said allocated data slots is referred to as a channel between the two users.

In such a network, so called switch nodes, each connected to one or more bitstreams, or fibers, are used to switch time slot data between different bitstreams. For example, a channel between a first and a second end users connected to a first and a second, respectively, node on a first and a second, respectively, fiber is defined by a first set of time slots on a bitstream propagating on the first fiber and a second set of slots on a bitstream propagating on the second fiber, and the switch node is then used to transfer or copy time slot data from time slots of the first set of slots to time slots of the second set of slots, or vice versa.

According to prior art, switch nodes in synchronous time division multiplexed networks use a control memory that maps each incoming slot number to the outgoing slot number. Such mapping may involve both a mapping in the time domain, i.e. control of the order in which time slot

data are written into each bitstream, and a mapping in the space domain, i.e. controlling which time slot data goes to which bitstream. For example, so called time-space-time (TST) switches are described in "Data and Computer Communications", 4th ed., by Williams Stallings, Macmillan Publishing Company. However, prior art switches all show limitation as to the possibilities of switching time slots in space and time. Also, prior art switches show limitations as to switching speed and capacity.

Objects of the invention

An object of the invention is therefore to provide a switch which provides greater freedom as to the possibilities of switching time slots in space and time.

Another object of the invention is to increase the switching speed and capacity.

Summary of the invention

According to a first aspect of the invention, the above mentioned objects are achieved by a method, in a switch node, of the kind set out in the introduction, wherein an isochronous channel is established on said first and second bitstreams, said channel comprising a first set of time slots in the first bitstream and a second set of time slots in the second bitstream, said method comprising the steps of: reading time slot data from a time slot of said first set of time slots in said first bitstream; identifying the channel associated with said time slot; mapping said time slot data to a time slot of said second bitstream based upon the identification of said channel, said time slot being a time slot of said second set of time slots; and writing said time slot data into said time slot in said second bitstream.

According to a second aspect of the invention, said objects are achieved by an apparatus of the kind set out in the introduction, wherein an isochronous channel is established on said first and second bitstreams, said

channel comprising a first set of time slots in the first bitstream and a second set of time slots in the second bitstream, said apparatus comprising: first bitstream access means for reading time slot data from a time slot of said first set of time slots in said first bitstream; identifying means for identifying the channel associated with said time slot; mapping means for mapping said time slot data to a time slot of said second bitstream based upon the identification of said channel, said time slot being a time slot of said second set of time slots; and second bitstream access means for writing said time slot data into said time slot in said second bitstream.

The invention is hence based upon the idea of transferring time slot data, belonging to a specific channel, or circuit, read from the first bitstream at an input port of said switch, to an output port of the switch without providing any direct specification of a time slot in the second bitstream into which the data shall be written. i.e. not having to specify , at channel set-up, a strictly unambiguous slot-to-slot mapping through the switch. Instead, resolution is achieved, generally in connection with the output port, by means of an identification of the channel. This provides the advantage that there is no need for any strict timing requirements between the individual time slots of a channel at the input port and the individual time slot of the corresponding channel at the output port, but the phase of the channel on one of the bitstreams may be arbitrary shifted in relation to the phase of the corresponding channel on another bitstream.

The mapping of time slot data to time slots based upon the identification of a channel preferably comprises mapping said time slot data to the next available time slot of said channel on said second bitstream. The advantage here lies in that there is no need to wait for a certain slot of the channel in the second bitstream. Instead, data is directly mapped to the first time slot

available to the channel that has not yet been filled with switched data.

The writing of said time slot data from time slots of said first set of time slots into time slots of said second set of time slots is preferably done in maintained mutual order. This is of course required in many applications, and when used in such a context the switch must be able to meet this requirement.

According to the invention, said read time slot data may be transferred within said node using allocated time slots of an internal bitstream, said bitstream being divided into cycles which in turn are divided into time slots. Optionally, said internal bitstream is shared by several input and output ports.

Such an internal bitstream simplifies the internal handling of the time slot data in the node. For example, if data is to be multicasted from one bitstream to several other bitstreams, there is no need to make copies of the data to be switched since it will be transferred to all parts of the node having connections with the other bitstreams. Also, this put less requirement on the switch internal operations to be synchronized to the external bitstreams. In fact, it enables the node to switch data asynchronously within the node. However, a synchronous operation is also preferred, depending on the actual application.

The channel identification is preferably achieved through associating said read time slot data with a channel identifier, where the association may for example be realized by a) associating information as to the position, in said first bitstream, of the time slot from which said time slot data was read with said channel identifier, b) associating information as to the position, in said internal bitstream, of the time slot in which said time slot data is transferred, with said channel identifier, or c) connecting said time slot data with a channel identifying header.

When connecting, or tagging, said time slot data with a channel identifying header, these are preferably transferred within said node using time slots of an internal bitstream of the kind described above. Said time slot data is either concatenated with said channel identifying header, whereupon they are transferred in the same time slot in the internal bitstream, or said time slot data is transferred in a time slot, in said internal bitstream, which has a predetermined position in relation to the time slot in which said connected channel identifying header is transferred.

According to a modification of the latter case, the channel identifier is transferred by a predefined parallel channel comprising one or more allocated time slots, i.e., in other words, the channel identifier is transferred using side-band signaling.

Of course, time slot data and the associated header may also be transferred within the node using private connections, multiplexors, or other transferring means.

According to another embodiment of the invention said step of mapping said time slot data to a time slot of said second bitstream based upon the identification of said channel comprises: addressing an entry in a channel-to-slot table using the identification of said channel as an address; reading information designating a time slot position in said second bitstream from said entry in said channel-to-slot table, said time slot position corresponding to a time slot of said second set of time slots; addressing an entry in a slot-to-next slot table using said information designating a time slot position; reading, from said entry in said slot-to-next slot table, information as to the position of the next time slot of said second set of slots in said second bitstream; writing said information as to the position of the next time slot into said channel-to-slot table at said entry in said channel-to-slot table to be used at the next addressing thereof; and writing the time slot data

associated with said identification into a time slot of the second bitstream having a position identified by either the time slot position read from said channel-to-slot table or the next time slot position read from said slot-to-next-slot table. This embodiment provides a preferable way of achieving the mapping of time slot data based upon the associated channel identifier.

According to yet another embodiment of the invention said step of mapping said time slot data to a time slot of said second bitstream based upon the identification of said channel comprises: selecting a channel specific FIFO buffer, based upon the identification of said channel; storing said time slot data in said selected channel specific FIFO buffer; and writing time slot data stored in said channel specific FIFO buffer into the time slots of said second set of time slots in the second bitstream. This embodiment provides an advantageous way of assuring that time slot data belonging to a certain channel is written to the first available time slot in the second set of time slots allocated to the channel on the second bitstream. Thus, it is not necessarily to wait for a particular time slot on the second bitstream into which the time slot data can be stored.

Another feature of the invention is that said time slot data from a time slot of said first set of time slots is switched to said second bitstream and to one or more further bitstreams, said channel comprising a respective set of time slots in each respective bitstream of said one or more further bitstreams, comprising: mapping said time slot data to a respective time slot of each respective one of said one or more further bitstreams based upon the identification of said channel; and writing said time slot data into the said respective time slot in the respective one of said one or more further bitstreams.

Thus, multicasting, or broadcasting, is easily provided.

A bitstream at an input port of the switch node may be terminated at the switch node, as is the case if the switch node is a tail end node, or it may continue past the switch node to reach other nodes located downstream with respect to the switch node. Also, a bitstream at an output port of the switch node may origin from the switch node, as is the case if the switch node is a head end node, or it may origin from other nodes located upstream with respect to the switch node.

Of course, the invention is not restricted to DTM networks but can be used in any circuit switched synchronous time division multiplexed network with cycles and slots of arbitrary sizes.

Furthermore, the present application forms one of a series of three applications referring to related inventive ideas, filed on the same day and having the same title, the descriptions of the other two thus hereby being incorporated by reference.

The above mentioned and other aspects and features of the invention will be more fully understood from the following description, with reference to the accompanying drawings, of exemplifying embodiments thereof.

Brief description of the drawings

Exemplifying embodiments of the invention will be described below with reference to the accompanying drawings, wherein:

Fig. 1 schematically shows the structure of a bit-stream of a circuit switched time division multiplexed network;

Fig. 2 schematically shows a switch node in a first embodiment of the invention;

Fig. 3 schematically shows a switch node in a second embodiment of the invention;

Fig. 4 schematically shows a switch node in a third embodiment of the invention;

Fig. 5 schematically shows a switch node in a fourth embodiment of the invention; and

Fig. 6a, 6b and 7 show different embodiments of the internal structure of the mapping means included in the switch node of the present invention.

Detailed description of preferred embodiments

With reference to Fig. 1, the structure of the time multiplexed bitstreams in a circuit switched synchronous time division multiplexing network, according to the present invention, is shown. The bandwidth of each wavelength, i.e. each bitstream, is divided into fixed length, for example 125 μs, cycles or frames. Each frame is in turn divided into fixed size, for example 64 bits, time slots. The number of time slots within a frame thus depends on the network's bit rate. Of course, the number of time slots 1-6 shown in the frame of the bitstream in Fig. 1 is merely illustrative, the actual number of slots within each frame being far greater.

The time slots are in general divided into two groups, control slots C and data slots D. The control slots C are used for control signaling between nodes of the network, i.e. for carrying messages between nodes for the internal operation of the network, such as for channel establishment, slot allocation, and the like. The data slots D are used for the transfer of user data between end users connected to said nodes.

In addition to said control slots and data slots, each cycle comprises one or more synchronization slots S used to synchronize the operation of each node in relation to each frame. Also, to make sure that the number of slots in one frame will not overlap a following frame, a guard band G is added after the last slot at the end of each frame. As indicated in Fig. 1, the bitstream cycle is repeated continuously.

Each node has access to at least one control slot C and to a dynamic number of data slots D on the bitstream

used by said node. Each node uses its control slot C to communicate with other nodes within the network. The number of data slots D allocated to each node depends upon the transfer capacity requested by the end users served by the respective node. If the end users of a certain node require a large transfer capacity, the node will allocate more data slots for that purpose. On the other hand, if the end users of a certain node merely requires a small transfer capacity, the node may limit its number of allocated data slots. Also, the number of control slots allocated to each node may be increased or decreased depending on the node's demand for signaling capacity. Hence, the allocation of both time slots and data slots to different nodes may by dynamically adjusted as the network load changes. It is understood, that in this kind of circuit switching there is no header or address information embedded in the data stream.

Note, that in the basic embodiment, a switch according to the invention does not handle control time slots C any differently than data time slot D. As far as the switch is concerned, both control slot and data slots provide time slot data to be switched in accordance with switching instructions stored in the switch. However, a switch node controller, controlling the operation of the switch may be allocated to use one or more control and data slots for receiving and/or transmitting information regarding channel establishment, modification and termination, and to control the switching instructions of the switch based thereupon.

Fig. 2 shows a switch node 210 connected to two unidirectional optical fibers 214 and 219 transferring a first bitstream 215 and a second bitstream 220, respectively. As previously stated, and also indicated in Fig. 2, each of the bitstreams is divided into cycles and each of said cycles is divided into time slots.

The node is by means of a Switch Node Controller (SNC) 235 configured to switch data from a specific set

of time slots in the frame transferred by the first bitstream to a specific set of time slots in the frame transferred by the second bitstream. At setup of a channel through the switch node, the SNC 235 is informed of which time slots in the first bitstream and which time slots in the second bitstream, respectively, that are allocated to the channel, or circuit. The SNC 235 is connected to a channel identifying table 240 and mapping means 250, both of which will be described below, the connection being illustrated in Fig. 2 with dotted lines.

The switch node includes first bitstream access means 225 for reading time slot data from time slots in said first bitstream. The first bitstream access means 225 includes a Medium Access Unit (MAU), a bit clock, a slot counter and a frame clock (neither of which is shown in the figure). The MAU enables the node to read the time slots being transferred by the first bitstream. The bit clock is synchronized to the bitrate of the bitstream 215 transferred by the fiber 214 and used as input to the slot counter. The slot counter counts the number of slots transferred by the fiber 214 and is cyclically restarted by the frame clock at the start of each new cycle.

At channel, or circuit, set-up the SNC 235 stores information in the channel identifying table 240 that for each time slot identifies a channel, or circuit. Each time slot in the first bitstream read by the MAU included in the first access means has a corresponding entry in said table, and each entry that represents a time slot carrying data to be switched by the switch node is associated with information for identifying the channel, or circuit, to which the time slot is allocated.

The counter value of the slot counter included in the first access means is used to address an entry in the channel identifying table 240. The information associated with the entry, which information in used for identifying a channel, is outputted from the table and transferred to the mapping means 250.

The mapping means, for example having the configuration as will be described later with reference to Fig. 6a and 6b, mapps time slot data to a position in a cycle, or frame, of the second bitstream 219, said position corresponding to one of the time slots of the channel in the second bitstream, and uses this position information to address the frame buffer 260. For each time slot read by the MAU that has information identifying a channel associated with it in the channel identifying table, the time slot data is transferred from the time slot of the first bitstream to the frame buffer 260, where it is stored at the address location given by the mapping means 250.

Included in the switch node are also second bitstream access means 230 for writing time slot data to time slots in said second bitstream. The second bitstream access means 230 includes a Medium Access Unit (MAU), a bit clock, a slot counter and a frame clock (neither of which is shown in the figure). The MAU enables the node to have access to the time slots being transferred by the second bitstream. The bit clock is synchronized to the bitrate of the bitstream 220 transferred by the fiber 219 and used as input to the slot counter. The slot counter counts the number of slots transferred by the fiber 214 and is cyclically restarted by the frame clock at the start of each new cycle. The counter value of the slot counter is used to address entries in the frame buffer 260. The time slot data stored in said frame buffer at a specific entry is transferred to the MAU, which MAU then writes the time slot data in a time slot having a position in a cycle of the second bitstream corresponding to the entry of the frame buffer.

In Fig. 2, two exemplifying channels, A and B, are to be switched by the switch node from bitstream 215 to bitstream 220. As can be seen in the table of the identifying means 240, the time slots numbered 1, 2 and 5 in the cycles of bitstream 215 are allocated to the channel

denoted A, and the data carried by these time slots are to be switched to three time slots, for example, the time slots numbered 2, 3 and 4, in the cycles of bitstream 220. The time slots numbered 3 and 7 in the cycles of bitstream 215 are allocated to channel B, and the data carried by these time slots are to be switched to two time slots, for example, the time slots numbered 1 and 5, in the cycles of bitstream 220. Since neither one of the time slots numbered 4 and 6 in the first bitstream is allocated to a channel to be switched by this switch node, the table does not contain any information identifying a channel for the corresponding entries.

In Fig. 2, only seven entries corresponding to cycles with seven time slots have been indicated in the channel identifying table 240, but, as described earlier with reference to Fig. 1, a cycle in a bitstream will in practice contain a far greater number of slots and, thus, the table a far greater number of corresponding entries.

When the first bitstream access means 225 reads time slot number 2 from a cycle of the first bitstream 215, its slot counter value will address the second entry of the channel identifying table 240. At this entry, information, in this case denoted A, identifying channel A, has been stored by means of the SNC 235 during circuit set-up. This information is thereby associated with time slot number 2, or with the data transferred by time slot number 2. Upon addressing the second entry, the information A, identifying channel A, will be outputted, and based upon this channel identifier A the mapping means 250 will output one of the time slots allocated to channel A in the second bitstream. In this case one of the three possible position numbers 2, 3 or 4 must be outputted, for example position number 3. The mapping means will use the position number to address the corresponding entry in the frame buffer 260, at which entry time slot data read from the first bitstream will be stored. Thus, the mapping means will in this case

address the third entry of the frame buffer 260, at which entry the data read by the first bitstream access means from time slot number 2 of the first bitstream will be stored. The first bitstream access means then continues to read time slot number 3 from the cycle of the first bitstream and its slot counter is incremented to address the third entry of the table of the channel identifying table 240. Upon addressing the third entry, information, in this case denoted B, identifying channel B will be outputted and used by the mapping means to output one of the position numbers 1 or 5 allocated to channel B in the second bitstream, for example position number 1. This position is then again used for addressing an entry of the frame buffer 260, at which entry the data read by the first bitstream access means from time slot number 3 of the first bitstream will be stored. This procedure is repeated continuously for all time slots of the first bitstream, at the start of each new cycle in the first bitstream the slot counter is restarted by the frame clock.

At the same time, the second bitstream access means 230 will write time slot data to time slots in the second bitstream. When its slot counter has been restarted by its frame clock at the start of a new cycle in the second bitstream, the counter value will be one, and the slot counter will address the first entry of the frame buffer 260. The data stored in the frame buffer at this first entry will be outputted and transferred to the MAU included in the second bitstream access means. The MAU will write the transferred data in the first time slot of the frame currently being transferred by the second bitstream. Thus, the data transferred by the third time slot in the first bitstream has now been switched to the first time slot in the second bitstream. The slot counter value is then incremented by one and the second entry of the frame buffer is addressed. The data stored at this second entry is transferred to the MAU and written into

the second time slot of the cycle being transferred by the second bitstream. After yet another incrementation of the slot counter value, the third entry of the frame buffer will be addressed. The data stored at this third entry is transferred to the MAU and written into the third time slot of the cycle being transferred by the second bitstream. Thus, the data transferred by the second time slot in the first bitstream has now been switched to the third time slot in the second bitstream. This procedure is repeated until the slot counter of the second bitstream access means is once again restarted by the frame clock.

In Fig. 3 a second embodiment of the invention is shown. The switch node 310 is again connected to two unidirectional optical fibers 314 and 319 transferring a first bitstream 315 and a second bitstream 320, respectively. The switch node includes first bitstream access means 325 and second bitstream access means 330. These fibers, bitstreams and access means correspond to the fibers, bitstreams and access means previously described with reference to Fig. 2 and any further description thereof is therefore omitted.

The switch node here includes a medium on which an internal bitstream 370 propagates. The internal bitstream, which is divided into cycles which in turn are divided into time slots, is used for transferring time slot data within the switch node.

At channel set-up the SNC 335 stores information in a slot mapping table 338 and a channel identifying table 340.

Each time slot in the first bitstream read by the MAU included in the first access means has a corresponding entry in the slot mapping table 338, and each entry that represents a time slot carrying data to be switched by the switch node is associated with position information for a time slot in the internal bitstream 370. In the channel identifying table 340, each entry corresponds

to a position of a time slot in the cycles of the internal bitstream 370. Associated with each entry of the channel identifying table 340, and thus with each cyclically occurring time slot position, is information for identifying a channel.

When, for example, the first bitstream access means 325 reads time slot number 5 from a cycle of the first bitstream 315, its slot counter value will address the fifth entry of the slot mapping table 338. At this entry, position information, in this case position number 4, has been stored by means of the SNC 335 during circuit set-up. Upon addressing the fifth entry, the position number 4 will be outputted and used to control that the data read from time slot number 5 of the cycle of the first bitstream is written into time slot number 4 of the cycle of the internal bitstream. In connection with the part of the switch that is connected to the second bitstream, the time slots of the internal bitstream are read. Upon reading, for example, time slot number 2, a pointer will address the second entry of the channel identifying table 340. At this entry, information, in this case denoted A, identifying the channel A has been stored by means of the SNC 335 during circuit set-up. This information is thereby directly associated with time slot number 2 of the internal bitstream, and indirectly, via the slot mapping table 338, associated with a time slot number of the first bitstream, in this case also number 2, or indirectly with the data transferred by time slot number 2 of the first bitstream. Upon addressing the second entry, the information A identifying channel A, will be outputted, and based upon this channel identifier A the mapping means 350 will output one of the time slots allocated to channel A in the second bitstream. For example, position number 3. The mapping means will use the position number to address the corresponding entry in the frame buffer 360, at which entry time slot data read from the internal bitstream will be stored. Thus, the mapping means will in

this case address the third entry of the frame buffer 360, at which entry the data read from time slot number 2 of the internal bitstream will be stored. Thus, the data transferred by the second time slot in the first set of time slots in the first bitstream has now, via the second time slot of the internal bitstream, been switched to the third time slot in the second set of time slots of the second bitstream. This procedure is repeated continuously. At the start of each new cycle in the first bitstream, the slot counter of the first bitstream access means is restarted by the frame clock. For each time slot read from the internal bitstream the pointer addressing the channel identifying table 340 is incremented by one. At the start of each new cycle in the internal bitstream, the pointer is resetted to address the first entry of said channel identifying table.

In Fig. 4 a third embodiment of the invention is shown. The switch node 410 is again connected to two unidirectional optical fibers 414 and 419 transferring a first bitstream 415 and a second bitstream 420, respectively. The switch node includes first bitstream access means 425 and second bitstream access means 430. These fibers, bitstreams and access means correspond to the fibers, bitstreams and access means previously described with reference to Fig. 2 and any further description thereof is therefore omitted.

The switch node here includes means for connecting time slot data with a channel identifier header, these connecting means having the reference numeral 442.

At channel set-up the SNC 435 stores information in a channel identifying table 440.

Each time slot in the first bitstream read by the MAU included in the first access means has a corresponding entry in the channel identifying table 440, and each entry that represents a time slot carrying data to be switched by the switch node is associated with information for identifying a channel.

When, for example, the first bitstream access means 425 reads time slot number 5 from a cycle of the first bitstream 415, its slot counter value will address the fifth entry of the channel identifying table 440. At this entry, information, in this case denoted A, identifying the channel A has been stored by means of the SNC 435 during circuit set-up. Upon addressing said entry of the channel identifying table, the channel identifying header A will be outputted and transferred to the connecting means 442. For each time slot read by the MAU that has information identifying a channel associated with it, i.e. a channel identifying header, the time slot data is transferred from the time slot of the first bitstream to the connecting means 442.

Hence, in this example, the time slot data read from time slot number 5 of the first set of time slots is also transferred to the connecting means 442. The connecting means 442 will then connect said channel identifying header with said time slot data. The header will then at a later step be used by the mapping means 450 to output one of the time slots allocated to channel A in the second set of time slots in the second bitstream, for example, time slot with number 3. The mapping means will use the position number to address the corresponding entry in the frame buffer 460, at which entry the time slot data connected to said header will be stored. Thus, the data transferred by the fifth time slot in the first set of time slots in the first bitstream has now, via the connecting means, been switched to the third time slot in the second set of time slots of the second bitstream. In correspondence with the previous embodiments, this procedure is repeated continuously.

In Fig. 5 a fourth embodiment of the invention is shown. The switch node 510 is here connected to three unidirectional optical fibers 514, 519 and 522 transferring a first bitstream 515, a second bitstream 520, and a third bitstream 523, respectively. The switch node inclu-

des first bitstream access means 525, second bitstream access means 530 and third bitstream access means 531. All of these fibers, bitstreams and access means are of the same nature and have the same functionality as the fibers, bitstreams and access means previously described with reference to Fig. 2 and any further description thereof is therefore omitted.

In this embodiment of the invention the switch node includes a channel identifying table 540; a medium on which an internal bitstream 570 propagates; a first and a second internal bitstream access means 545 and 546; two sets of mapping means 550 and 551; and two sets of frame buffers 560 and 561. The internal bitstream is used for transferring time slot data within the switch node, and it propagates on said medium within the node in such way that it can be accessed in connection with those parts of the switch node that are connected to the node external bitstreams. The mapping means 550 and 551 and the frame buffers 560 and 561 are of the same kind as those described in connection with the previous first to third embodiments.

The first internal bitstream access means 545, having read access to the internal bitstream, is situated in connection with the part of the switch that is connected to the second bitstream. Correspondingly, the second internal bitstream access means, having read access to the internal bitstream, is situated in connection with the part of the switch connected to the third bitstream.

At channel set-up the SNC 535 stores information in the channel identifying table 540 and the two mapping means 550 and 551. The information stored in the mapping means may be chosen in such way that the switch node multicasts time slot data from the first bitstream to the second and the third bitstream.

For example, when the first bitstream access means 525 reads time slot number 5 from a cycle of the first bitstream 515, its slot counter value will address the

fifth entry of the channel identifying table 540. At this entry, information, in this case denoted A, identifying the channel A has been stored by means of the SNC 535 during circuit set-up. This information is thereby associated with time slot number 5, or with the data transferred by time slot number 5. Upon addressing the fifth entry of the channel identifying table, a channel identifying header A will be outputted and transferred to a time slot of the internal bitstream. The time slot data read from time slot number 5 by the first bitstream access means is also transferred to a time slot of the internal bitstream. The header is either concatenated with the slot data and stored in the same time slot of the internal bitstream, or the header and the slot data are stored in two separate time slots being separated with a predefined number of slots, or the header is transferred using a separate channel on said internal bitstream.

At a later step, when the first internal bitstream access means 545 read a header, for example, header A, and its connected time slot data from time slots of the internal bitstream, the header will be further transferred to the mapping means 550. The header will then be used by the mapping means 550 to output one of the time slots allocated to channel A in the second bitstream, for example, time slot with position number 3. The mapping means will use the position number to address the corresponding entry in the frame buffer 560. The time slot data connected to said header will be transferred from the first internal bitstream access means and stored in the frame buffer at said entry.

Correspondingly, when the second internal bitstream access means read a header, for example, header A, and its connected time slot data from the internal bitstream, the header will be used by the mapping means 551 to output one of the time slots allocated to channel A in

the third bitstream, for example, time slot with position number 2.

Thus, the data transferred by the fifth time slot in the first set of time slots in the first bitstream has now, via the internal bitstream, been switched to the third time slot in the second set of time slots of the second bitstream and to the second time slot in a third set of time slots of the third bitstream, and thereby multicasting has been realized. Of course, if either one of the mapping means 550 or 551 is configured with information that does not output a time slot position number on the basis of the header A, multicast will not be realized for channel A.

With reference to Fig. 6a and 6b, a principle structure of an embodiment of the mapping means according to the present invention, which for example may be the mapping means 250, 350, 450, 550, or 551 shown in the preceding figures, will now be described. The mapping means 650 basically includes two tables, a channel-to-slot table 640 and a slot-to-next slot table 660. At channel set-up, the SNC stores information in the channel-to-slot table and in the slot-to-next slot table. The channel-to-slot table has entries that are addressed by the information identifying a channel. Each entry of the channel-to-slot table 640 contains time slot position data referring to an entry of the slot-to-next slot table 660. In turn, each entry of the slot-to-next slot table contains data referring to a time slot position number in the second set of time slots in the second bitstream, said time slot position number corresponding to the position of the next time slot of the channel in a round-robin fashion. Said data of the slot to next slot table 660 is, upon addressing the corresponding entry, written back to the entry currently being addressed in the channel-to-slot table 640.

The mapping means 650 uses the time slot position number to address the frame buffer, as described herein.

The time slot position number is either outputted to the frame buffer from an entry of the channel-to-slot table 640, as shown in Fig. 6a, or from an entry of the slot-to-next slot table 660, as shown in Fig. 6b.

For example, assume that the time slots numbered 2, 3 and 4 have been allocated to a channel A, and the time slots numbered 1 and 5 have been allocated to a channel B, on the second bitstream. The information written by the SNC in the tables in accordance with these allocations are shown in the figures 6a and 6b.

Referring to Fig. 6a, the first time the channel-to-slot table 640 is addressed by a channel identifier denoted A, the entry corresponding to this identifier will output data that addresses the fourth entry of the slot-to-next slot table 660. The data at this fourth entry will be written back to the channel-to-slot table 640 at the entry given by channel identifier A. The data at this fourth entry is however also used for addressing the frame buffer. The next time the channel-to-slot table 640 is addressed by a channel identifier denoted A, the same entry of the channel-to-slot table will be addressed, but the data outputted will address the second entry of the slot-to-next slot table, and so on. This process is repeated continuously and, thus, the mapping means forms an indefinite linked list of time slot positions, 2, 3, 4, 2, 3..., and so on, to be used when addressing the frame buffer based on the channel identifier A. The linked list formed for channel B, will correspondingly be 1, 5, 1, 5..., and so on.

Now referring to Fig. 6b, the first time the channel-to-slot table 640 is addressed by a channel identifier denoted A, the entry corresponding to this identifier will output data that addresses the second entry of the slot-to-next slot table 660. The data used for addressing this second entry is however also used for addressing the frame buffer. The data at the second entry of the slot-to-next slot table will be read and written

back to the channel-to-slot table 640 at the entry given by channel identifier A. The next time the channel-to-slot table 640 is addressed by a channel identifier denoted A, the same entry of the channel-to-slot table will be addressed, but the data outputted will address the third entry of the slot-to-next slot table, and so on. Thus, the linked lists formed by the mapping means for the channel A and B are also in this case 2, 3, 4, 2, 3..., and, 1, 5, 1, 5..., respectively.

Referring now to Fig. 7, a principle structure of yet another embodiment of the mapping means according to the present invention, which for example may be the mapping means 250, 350, 450, 550 or 551 shown in the preceding figures, will be described. The mapping means 750 includes a set of channel specific FIFO buffers 780, a FIFO buffer selection means 770 and a slot-to-channel mapping table 790. At channel set-up, the SNC stores information in the slot-to-channel mapping table.

Each FIFO buffer in the set of channel specific FIFO buffers corresponds to a respective channel and each buffer temporarily stores time slot data associated with a respective channel.

Upon receiving a channel identifier, the FIFO buffer selection means selects in which FIFO buffer, out of the set of FIFO buffers, the time slot data associated with said channel identifier is to be stored. This is accomplished by enabling the particular FIFO buffer to accept said time slot data presented to it.

The slot-to-channel mapping table has entries that are addressed by position information, which position information corresponds to time slots positions in the second set of time slots on the second bitstream. The position information is preferably generated by the slot counter of the bitstream access means 230, 330, 430, 530 and 531. Each entry of said table contains channel identifiers, or FIFO buffer identifiers, used for enabling the reading of a specific buffer as indicated by

said identifier. As a result of addressing the slot-to-channel mapping table with a certain position number, time slot data will be read from the FIFO buffer storing time slot data belonging to the channel to which the time slot with the corresponding position in the second set of the second bitstream is allocated to. This time slot data is then outputted from the mapping means, however, if the FIFO buffer in question is empty, the mapping means will output idle slot data. The time slot data, or idle slot data is then transferred directly to the bitstream access means or to a frame buffer.

It should be understood that with the embodiment of the mapping means as shown in Fig. 7, the operation of the frame buffer 260, 360, 460, 560 and 561 as previously described will be slightly different. The frame buffer is either completely omitted, whereupon the mapping means is directly connected to the bitstream access means 230, 330, 430, 530 and 531, for transferring time slot data thereto, or the frame buffer will be addressed by the slot counter of said bitstream access means rather than by the mapping means and receive the time slot data to be stored from the mapping means.

As is understood, the description above of exemplifying embodiments of the invention has been made in order to provide a better understanding thereof. Of course, an actual switch will incorporate elements not shown in the figures, and may also be realized using other components than the ones specifically described herein. For example, at different locations in the switch, further frame buffers, multiplexing means, and the like, may be provided to facilitate the desired operation.

As is understood by those skilled in the art, even though the invention has been described with reference to exemplifying embodiments thereof, different alterations and combinations may be made thereof within the scope of the invention, which is defined by the accompanying claims.

CLAIMS

1. A method for switching data, in a switch node, at least from a first bitstream to a second bitstream of a circuit switched synchronous time division multiplexing network, each of said bitstreams being divided into cycles and each of said cycles being divided into time slots, wherein an isochronous channel is established on said first and second bitstreams, said channel comprising a first set of time slots in the first bitstream and a second set of time slots in the second bitstream, said method comprising the steps of:

reading time slot data from a time slot of said first set of time slots in said first bitstream;

identifying the channel associated with said time slot;

mapping said time slot data to a time slot of said second bitstream based upon the identification of said channel, said time slot being a time slot of said second set of time slots; and

writing said time slot data into said time slot in said second bitstream.

2. A method as claimed in claim 1, said mapping step comprising mapping said time slot data to the next available time slot of said channel on said second bitstream.

3. A method as claimed in claim 1 or 2, comprising writing said time slot data from time slots of said first set of time slots into time slots of said second set of time slots in maintained mutual order.

4. A method as claimed in any one of the preceding claims, comprising the step of associating said read time slot data with a channel identifier and mapping said read

time slot data to a time slot of said second bitstream based upon said channel identifier.

5. A method as claimed in claim 4, wherein said step of associating said time slot data with said channel identifier comprises associating information as to the position, in said first bitstream, of the time slot from which said time slot data was read with said channel identifier.

6. A method as claimed in claim 4, wherein said read time slot data is transferred within said node using allocated time slots of an internal bitstream, said bitstream being divided into cycles which in turn are divided into time slots, and wherein said step of associating said time slot data with said channel identifier comprises associating information as to the position, in said internal bitstream, of the time slot in which said time slot data is transferred, with said channel identifier.

7. A method as claimed in claim 4, wherein said step of associating said time slot data with a channel identifier comprises connecting said time slot data with a channel identifying header.

8. A method as claimed in claim 7, wherein said time slot data and the connected channel identifying header are transferred within said node using time slots of an internal bitstream.

9. A method as claimed in claim 8, wherein said time slot data is transferred in a time slot, in said internal bitstream, which has a predetermined position in relation to the time slot in which said connected channel identifying header is transferred.

10. A method as claimed in claim 7 or 8, wherein said time slot data is concatenated with said channel identifying header.

11. A method as claimed in any of the preceding claims, wherein said step of mapping said time slot data to a time slot of said second bitstream based upon the identification of said channel comprises:

addressing an entry in a channel-to-slot table using the identification of said channel as an address;

reading information designating a time slot position in said second bitstream from said entry in said channel-to-slot table, said time slot position corresponding to a time slot of said second set of time slots;

addressing an entry in a slot-to-next slot table using said information designating a time slot position;

reading, from said entry in said slot-to-next slot table, information as to the position of the next time slot of said second set of slots in said second bitstream;

writing said information as to the position of the next time slot into said channel-to-slot table at said entry in said channel-to-slot table to be used at the next addressing thereof; and

writing the time slot data associated with said identification into a time slot of the second bitstream having a position identified by either the time slot position read from said channel-to-slot table or the next time slot position read from said slot-to-next-slot table.

12. A method as claimed in any one of claims 1-10, wherein said step of mapping said time slot data to a time slot of said second bitstream based upon the identification of said channel comprises:

selecting a channel specific FIFO buffer, based upon the identification of said channel;

storing said time slot data in said selected channel specific FIFO buffer; and

writing time slot data stored in said channel specific FIFO buffer into the time slots of said second set of time slots in the second bitstream.

13. A method as claimed in any one of the preceding claims, wherein said time slot data from a time slot of said first set of time slots is switched to said second bitstream and to one or more further bitstreams, said channel comprising a respective set of time slots in each respective bitstream of said one or more further bitstreams, comprising:

mapping said time slot data to a respective time slot of each respective one of said one or more further bitstreams based upon the identification of said channel; and

writing said time slot data into the said respective time slot in the respective one of said one or more further bitstreams.

14. A method as claimed in any one of the preceding claims, wherein channel management is provided by the dynamic allocation and deallocation of time slots in accordance with changing user capacity requirements.

15. An apparatus for switching data at least from a first bitstream to a second bitstream of a circuit switched synchronous time division multiplexing network, each of said bitstreams being divided into cycles and each of said cycles being divided into time slots, wherein an isochronous channel is established on said first and second bitstreams, said channel comprising a first set of time slots in the first bitstream and a second set of time slots in the second bitstream, comprising:

first bitstream access means (225; 325; 425; 525) for reading time slot data from a time slot of said first set of time slots in said first bitstream;

identifying means (240; 340; 440; 540) for identifying the channel associated with said time slot;

mapping means (250; 350; 450; 550, 551; 650; 750) for mapping said time slot data to a time slot of said second bitstream based upon the identification of said channel, said time slot being a time slot of said second set of time slots; and

second bitstream access means (230; 330; 430; 530, 531) for writing said time slot data into said time slot in said second bitstream.

16. An apparatus as claimed in claim 15, wherein said mapping means is arranged to mapp said time slot data to the next available time slot of said channel on said second bitstream.

17. An apparatus as claimed in claim 15 or 16, wherein said mapping means is arranged to mapp said time slot data to time slots in such a way that said time slot data from time slots of said first set of time slots are written into time slots of said second set of time slots in maintained mutual order.

18. An apparatus as claimed in any one of claims 15-17, wherein said identifying means comprises associating means for associating said read time slot data with a channel identifier and wherein said mapping means comprises means for mapping said read time slot data to a time slot of said second bitstream based upon said channel identifier.

19. An apparatus as claimed in claim 18, wherein said associating means comprises means for associating information as to the position, in said first bitstream,

of the time slot from which said time slot data was read with said channel identifier.

20. An apparatus as claimed in claim 18, comprising a medium (370; 570) for the transfer of said read time slot data within said apparatus in allocated time slots in an internal bitstream propagation on said medium, wherein said internal bitstream is divided into cycles which in turn are divided into time slots, and wherein said associating means comprises means for associating information as to the position, in said internal bitstream, of the time slot in which said time slot data is transferred, with said channel identifier.

21. An apparatus as claimed in claim 18, wherein said associating means comprises means (442) for connecting said time slot data with a channel identifying header.

22. An apparatus as claimed in claim 21, wherein said time slot data and the connected channel identifying header is transferred within said node using time slots of an internal bitstream.

23. An apparatus as claimed in claim 22, wherein said time slot data is transferred in a time slot, in said internal bitstream, which has a predetermined position in relation to the time slot in which said connected channel identifying header is transferred.

24. An apparatus as claimed in claim 21 or 22, wherein means for connecting said time slot data with a channel identifying header is arranged to concatenate said time slot data with said channel identifying header.

25. An apparatus as claimed in any one of claims 15-24, wherein said mapping means comprises:

a channel-to-slot table (640) having entries which are addressable using the identification of said channel as address and which provide information, at the respective entry, as to a respective time slot position of a time slot of said second set of time slots in said second bitstream; and

a slot-to-next slot table (660) having entries which are addressable using said information as to a time slot position of a time slot of said second set of time slots and which provides information, at each respective entry, as to the position of the next time slot of said second set of slots in said second bitstream.

26. An apparatus as claimed in claim 25, said mapping means further comprising means for addressing an entry in said channel-to-slot table, for reading information designating a time slot position from said entry in said channel-to-slot table for addressing an entry in said slot-to-next slot table using said information designating a time slot position, for reading, from said entry in said slot-to-next slot table, information as to the position of the next time slot of said second set of slots in said second bitstream, for writing said information as to the position of the next time slot into said channel-to-slot table at said entry in said channel-to-slot table to be used at the next addressing thereof, and for writing the time slot data associated with said identification into a time slot of the second bitstream having a position identified by either the time slot position read from said channel-to-slot table or the next time slot position read from said slot-to-next-slot table.

27. An apparatus as claimed in any one of claims 15-24, wherein said mapping means comprises:

a set of channel specific FIFO buffers (780), each FIFO buffer corresponding to a respective channel and

each FIFO buffer temporarily storing time slot data associated therewith;

a FIFO buffer selection means (770) for selecting in which FIFO buffer to store said time slot data based upon said channel identification; and

a slot-to-channel mapping table (790) providing information, for at least each time slot of said second set of time slots on said second bitstream, as to which FIFO buffer to be selected for transmission of time slot data to the second bitstream.

28. An apparatus as claimed in any one of claims 15-27, wherein said first set of time slots is also switched to one or more further bitstreams, said channel comprising a respective set of time slots in each respective bitstream of said one or more further bitstreams, said apparatus comprising:

means for mapping said time slot data to a respective time slot of each respective one of said one or more further bitstreams based upon the identification of said channel; and

means for writing said time slot data into the said respective time slot in the respective one of said one or more further bitstreams.

29. An apparatus as claimed in any one of claims 15-28, wherein channel management is provided by the dynamic allocation and deallocation of time slots in accordance with changing user capacity requirements.

ABSTRACT

The present invention refers to a method and an apparatus for switching data at least from a first bitstream to a second bitstream of a circuit switched time division multiplexed network, each of said bitstreams being divided into cycles and each of said cycles being divided into time slots.

The invention comprises reading time slot data from a time slot of a first set of time slots allocated to a channel in said first bitstream; identifying the channel associated with said time slot; mapping said time slot data to a time slot of said second bitstream based upon the identification of said channel, said time slot being a time slot of a second set of time slots allocated to the channel in said second bitstream; and writing said time slot data into said time slot in said second bitstream.

(Elected for publication: Fig. 2)

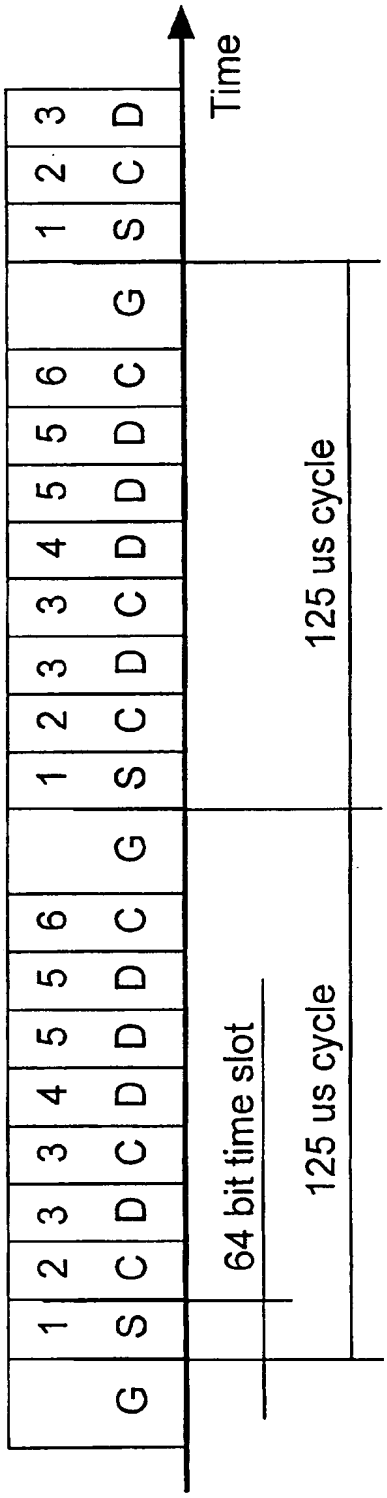
Time
G
1
S
2
C
3
D
3
C
4
D
5
D
5
D
6
C
G
1
S
2
C
3
D
3
C
4
D
5
D
5
D
6
C
G
1
S
2
C
3
D
64 bit time slot
125 us cycle
125 us cycle

FIG. 1

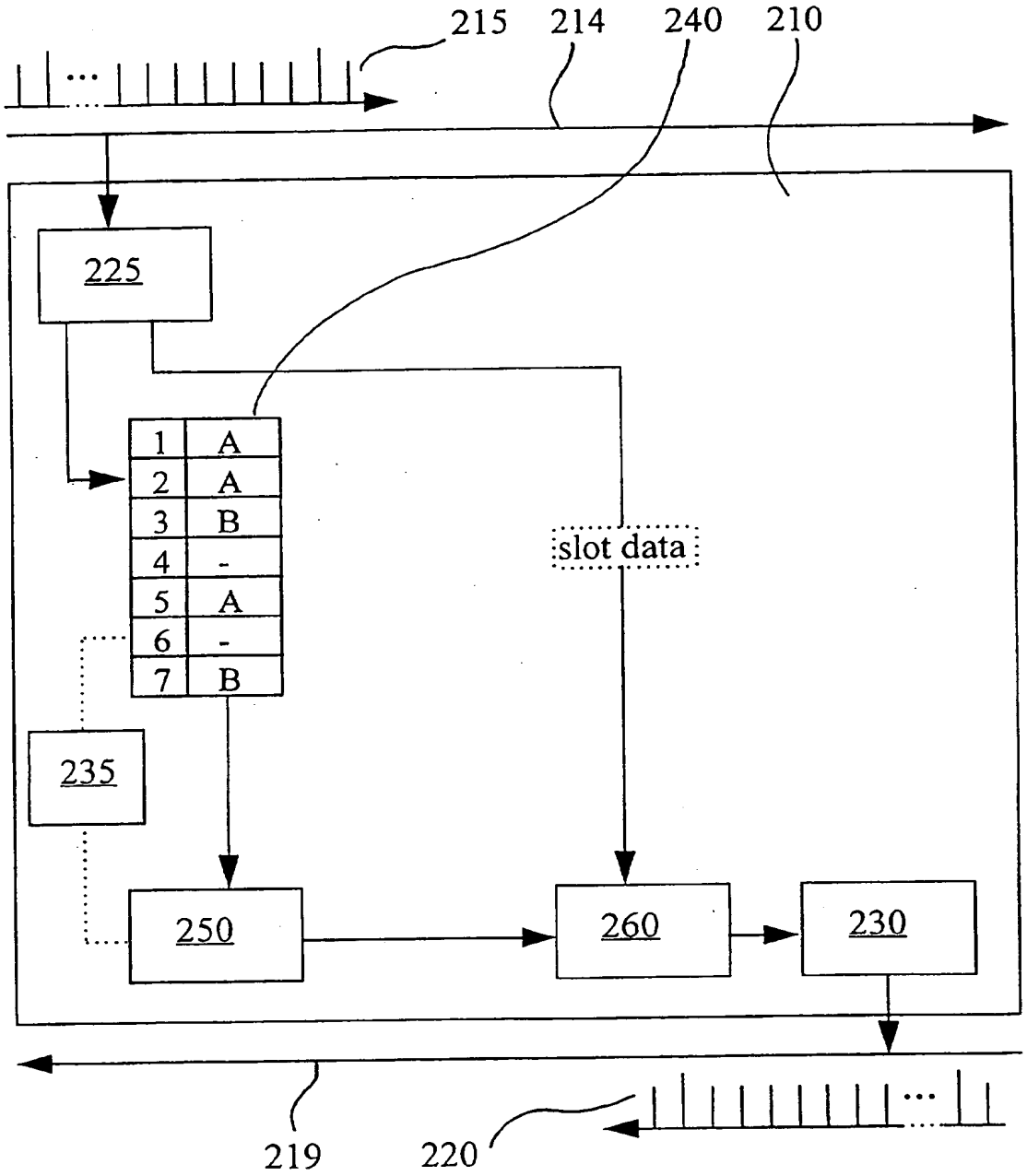
215
214
240
210
225
1 A
2 A
3 B
4 -
5 A
6 -
7 B
slot data
235
250
260
230
219
220

FIG. 2

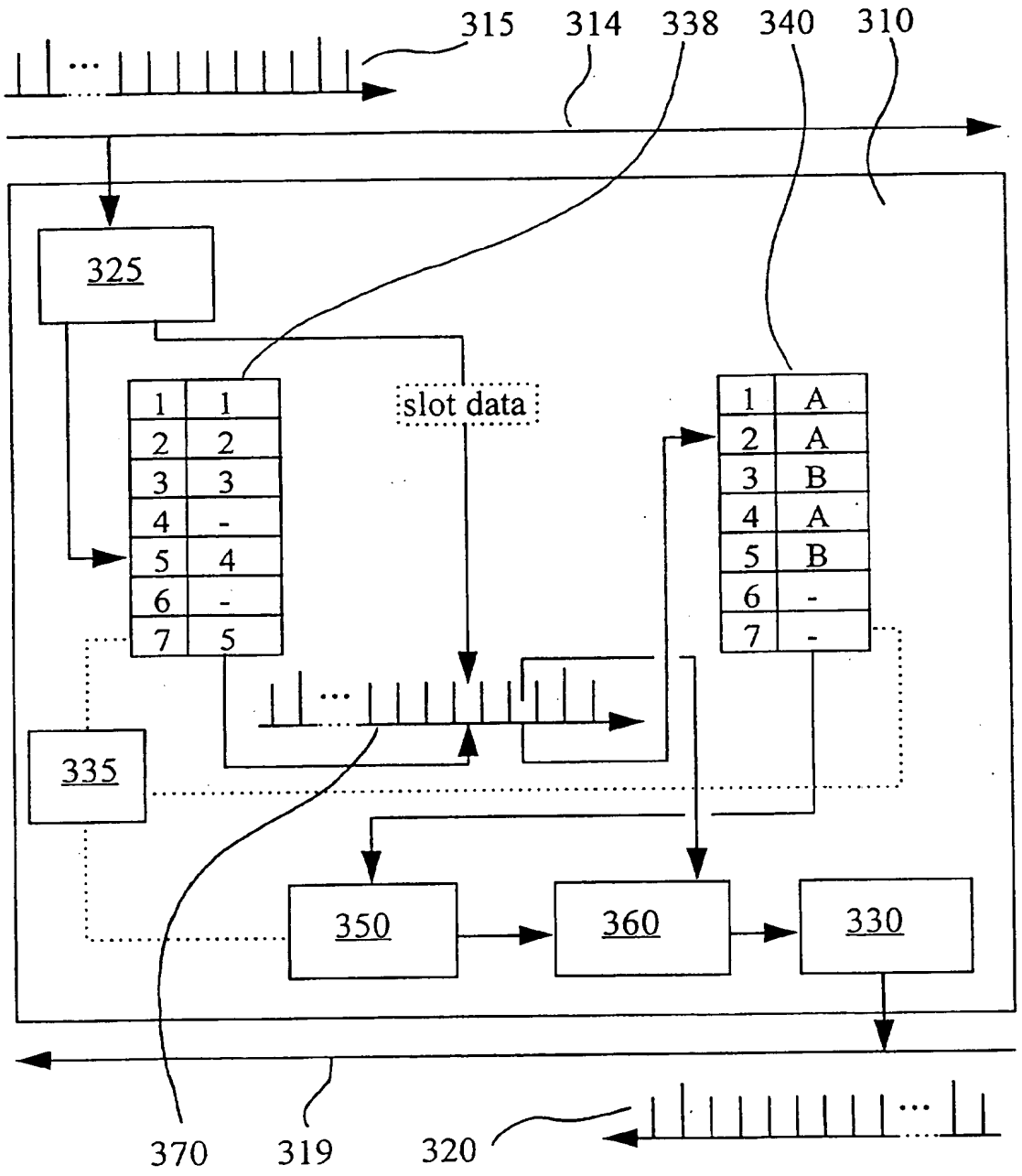
315
314
338
340
310
325
1 1
2 2
3 3
4 -
5 4
6 -
7 5
slot data
1 A
2 A
3 B
4 A
5 B
6 -
7 -
335
350
360
330
370
319
320

FIG. 3

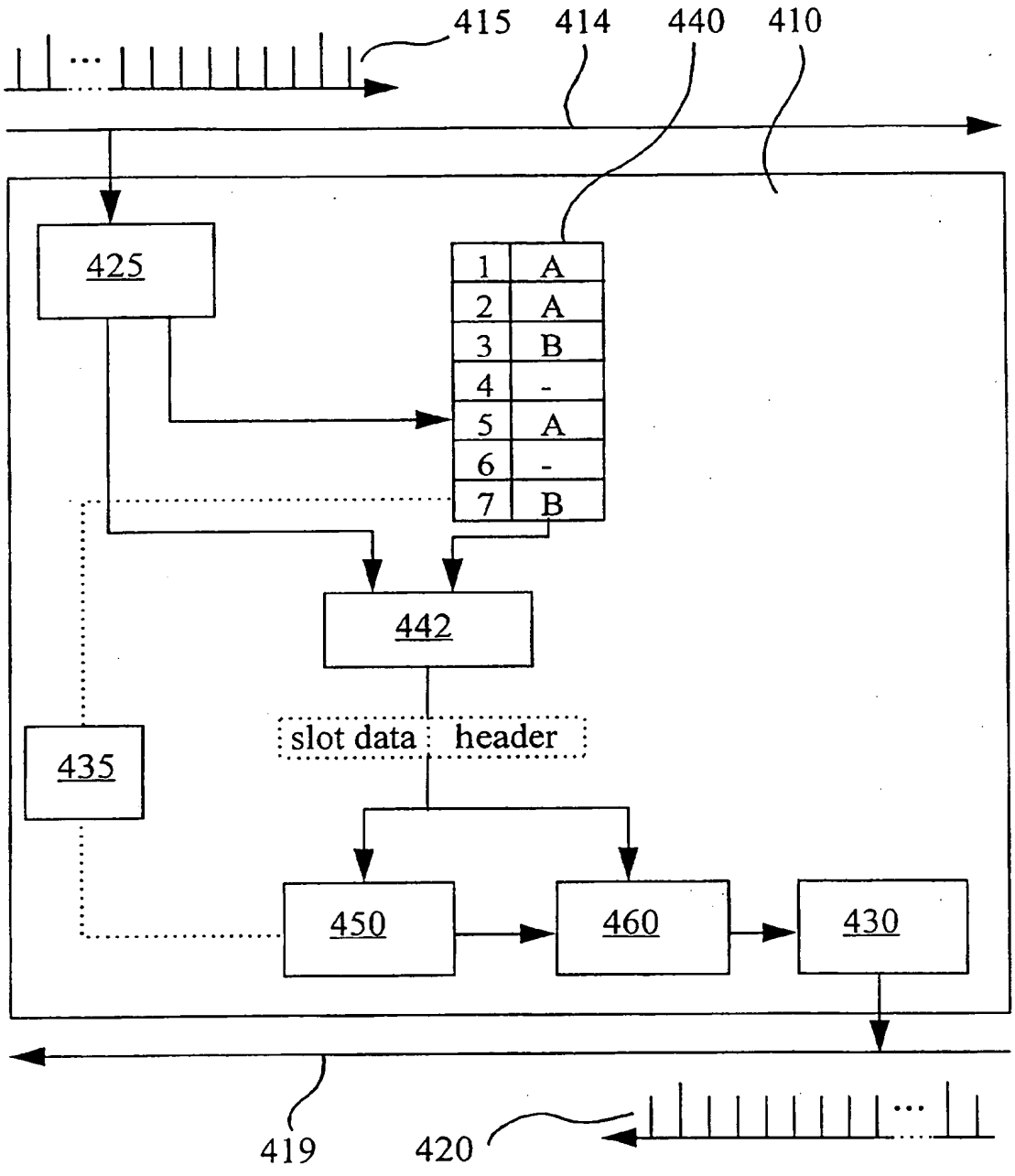
415
414
440
410
425
1 A
2 A
3 B
4 -
5 A
6 -
7 B
442
slot data
header
435
450
460
430
419
420

FIG. 4

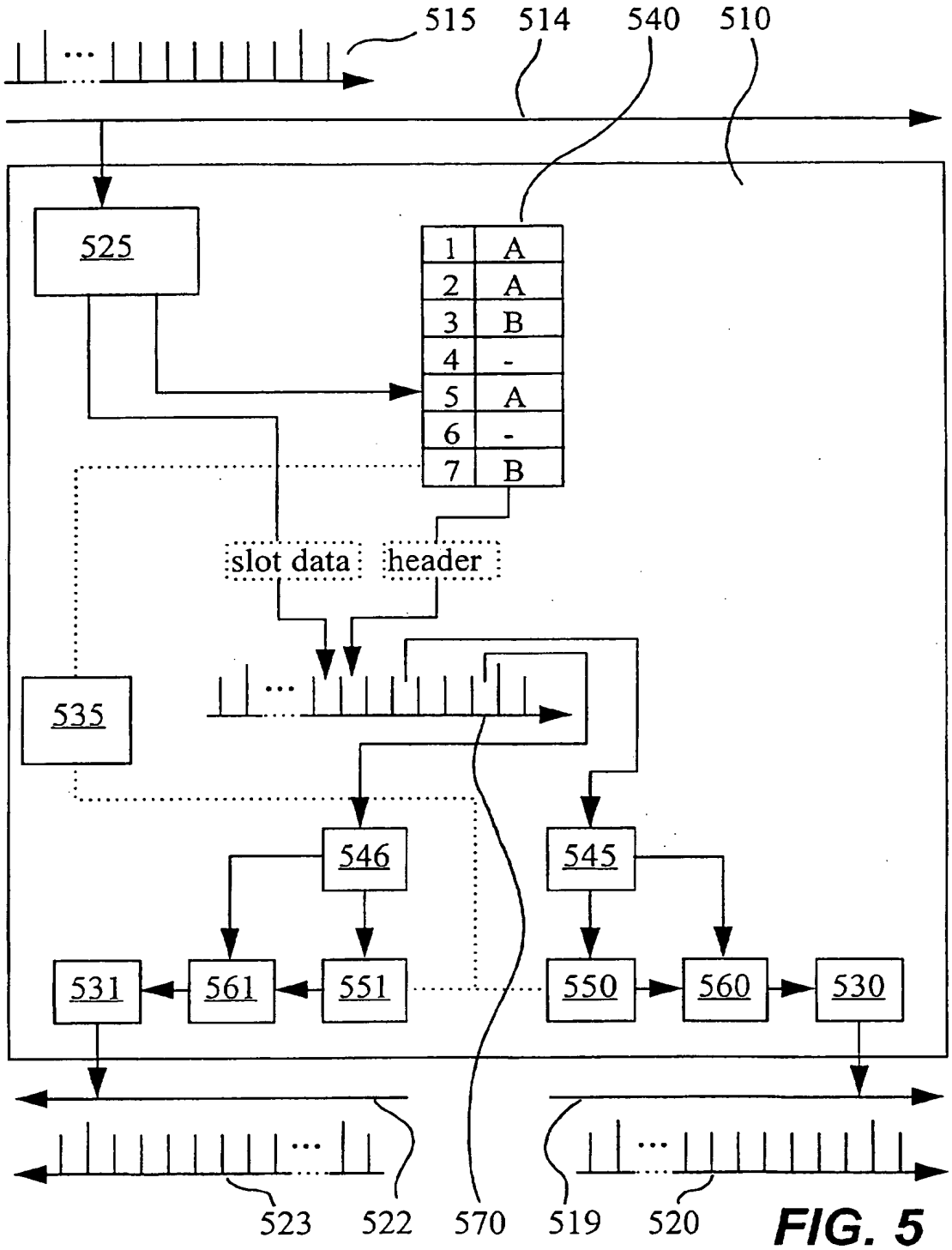
515
514
540
510
525
1 A
2 A
3 B
4 -
5 A
6 -
7 B
slot data
header
535
546
545
531
561
551
550
560
530
523
522
570
519
520

FIG. 5

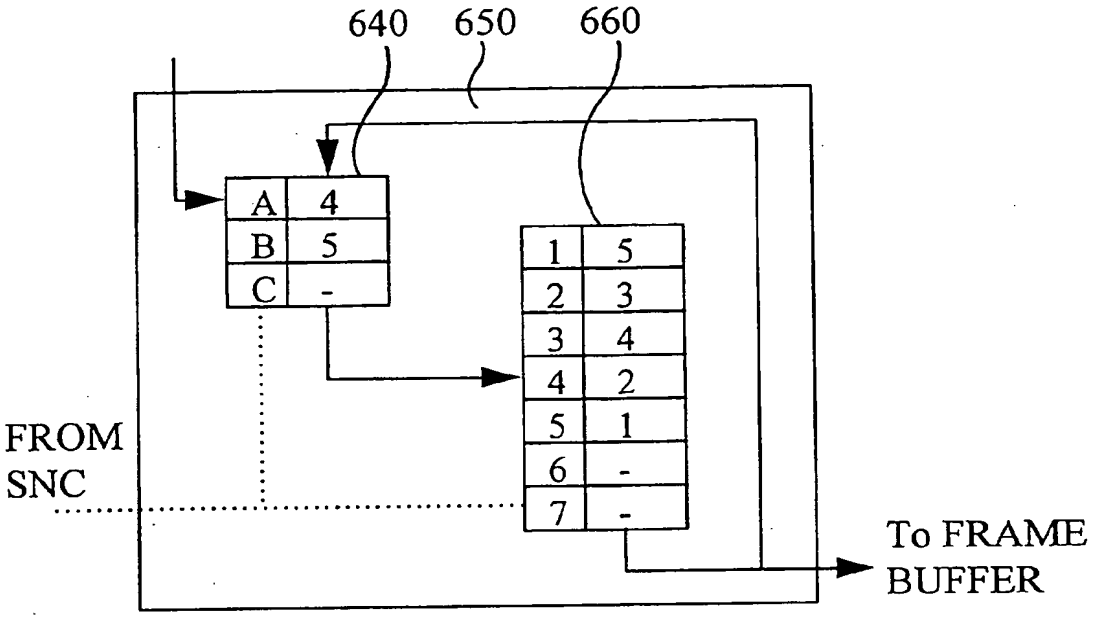
640
650
660
A 4
B 5
C -
1 5
2 3
3 4
4 2
5 1
6 -
7 -
FROM SNC
To FRAME BUFFER

FIG. 6a

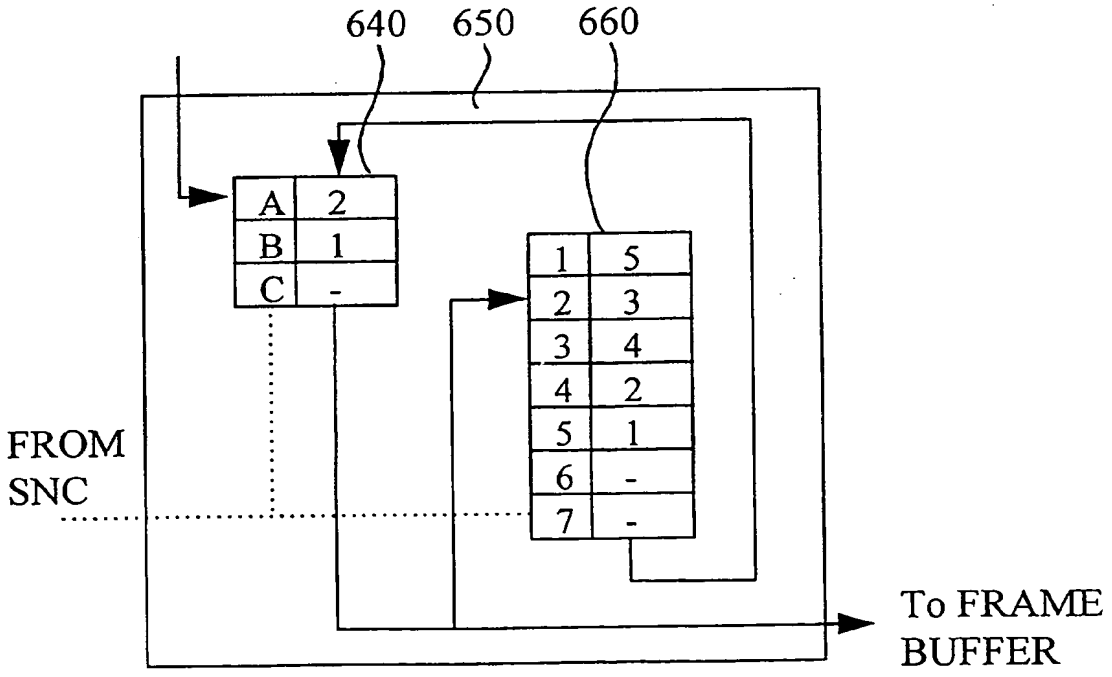
640
650
660
A 2
B 1
C -
1 5
2 3
3 4
4 2
5 1
6 -
7 -
FROM SNC
To FRAME BUFFER

FIG. 6b

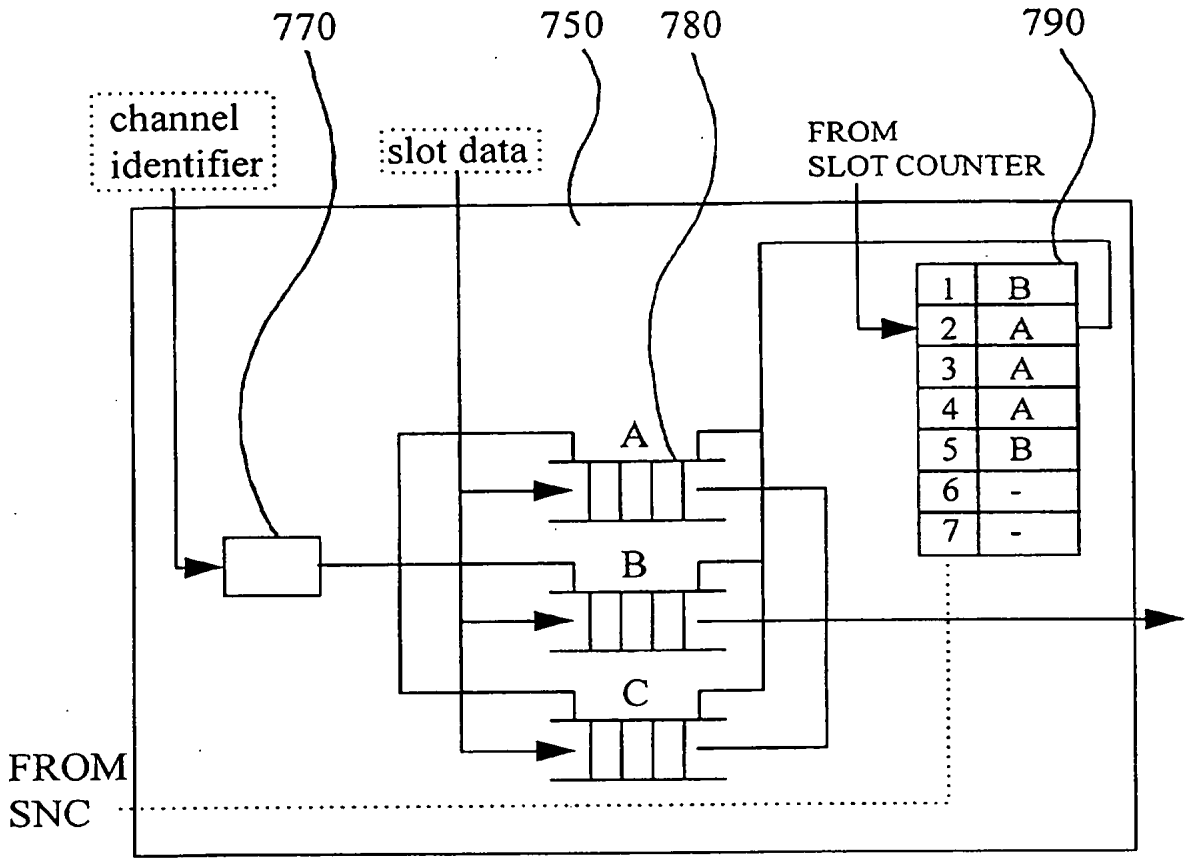
770
750
780
790
channel identifier
slot data
FROM SLOT COUNTER
1 B
2 A
3 A
4 A
5 B
6 -
7 -
A
B
C
FROM SNC

FIG. 7